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Date: November 23, 2009 **Time Sent:**

To:	**Company:**	**Facsimile No:**	**Telephone No:**
Examiner Steve Theriault	US Patent and Trademark Office	571-273-5867	

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Sent By:	Matilda Mason	*Direct Phone:*	202-756-8661
Client/Matter/Tkpr:	067471-0011/5328	*Original to Follow by Mail:*	No
		Number of Pages, Including Cover:	36

Re: **Application Serial No. 10/720,030**
Attorney Docket No.: 067471-0030

Message:
Further to our telephone conversation, as requested please find attached the copies of Issue Fee Payment, Notice of Allowance, Amendment filed April 23, 2001, and the Office Action dated February 14, 2001 for Application Serial No. 09/280,777.

Main Facsimile: +1 202 756 8087 Facsimile Operator: +1 202 756 8090

U.S. practice conducted through McDermott Will & Emery LLP.
600 Thirteenth Street, N.W. Washington, D.C. 20005-3096 Telephone: +1 202 756 8000

NAK1-BG43

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Taketo Heishi et al.

Serial No.: 09/280,777

Filed: March 29, 1999

Title: INSTRUCTION CONVERTING APPARATUS USING PARALLEL EXECUTION CODE

Batch No.: G28

Examiner: D. Pan
Group Art Unit: 2183

June 22, 2001

Irvine, California 92614

ISSUE FEE TRANSMITTAL

Box Issue Fee
Assistant Commissioner of Patents
Washington, DC 20231

Dear Sir:

Enclosed is our check for $1,240.00 in payment of the Issue Fee for the above-identified application.

Please charge any additional fees to our deposit account No. 16-2462. A copy of this letter is enclosed for that purpose.

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Box Issue Fee, Assistant Commissioner for Patents, Washington, DC 20231, on June 22, 2001, by Daniel Kerby

Signature

June 22, 2001
Date of Signature

Very truly yours,

PRICE AND GESS

Joseph W. Price, Reg. No. 25,124
2100 S.E. Main St., Ste. 250
Irvine, CA 92614
949/261-8433

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with a[illegible]e fees, to: **Box ISSUE FEE**
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Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

TM02/0514

JOSEPH W PRICE
PRICE GESS & UBELL
2100 S E MAIN STREET STE 250
IRVINE CA 92614

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the ~~Box Issue Fee~~ address above on the date indicated below.

Daniel Kerby (Depositor's name)

(Signature)

June 22, 2001 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/280,777	03/29/99	033	PAN, D 2183	05/14/01

First Named Applicant: HEISHI, 35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION: INSTRUCTION CONVERTING APPARATUS USING PARALLEL EXECUTION CODE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
0 NAK1-BG43	712-212.000	G28	UTILITY	NO	$1240.00	08/14/01

1. Change of correspondence address or indication of " Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" Indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 PRICE AND GESS
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
(B) RESIDENCE: (CITY & STATE OR COUNTRY)
OSAKA, JAPAN

Please check the appropriate assignee category indicated below (will not be printed on the patent)
☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):
☒ Issue Fee
☐ Advance Order - # of Copies

4b. The following fees or deficiency in these fees should be charged to:
DEPOSIT ACCOUNT NUMBER 16-2462
(ENCLOSE AN EXTRA COPY OF THIS FORM)
☒ Issue Fee
☐ Advance Order - # of Copies

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) (Date) 6/22/2001

NOTE: The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

TM01/0514

JOSEPH W. PRICE
PRICE GESS & UBELL
2100 S E MAIN STREET STE 250
IRVINE CA 92614

RESPONSE DUE 8-14-01
ACTION Issue Fee

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/280,777	03/29/99	030	PAN, D 2193	05-14/01
First Named Applicant	HETHERINGTON	35 USC 154(b) term ext. =	0 Days.	

TITLE OF INVENTION: INSTRUCTION CONVERTING APPARATUS USING PARALLEL EXECUTION CODE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
0 NAP1-B643	712-212.000	628	UTILITY	NO	$1240.00	08/14/01

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

YOUR COPY

PTOL-85 (REV. 10-98) Approved for use through 09/30/99. OMB 0651-0033

Notice of Allowability

Application No.	Applicant(s)
09/280,777	Heishi et al.
Examiner	**Art Unit**
Pan	2183

–The MAILING DATE of this communication appears on the cover sheet with the correspondence address–

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 04/26/01*

2. ☒ The allowed claim(s) is/are *1,3-8,10-14,16-36 (claims 2,9,15 have been canceled)*

3. ☒ The drawings filed on *Jun 10, 1999* / ✓ are acceptable as formal drawings. *Applicant English translation of drawings filed on 03 17 99*

4. ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

   a) ☒ All b) ☐ Some* c) ☐ None of the:

   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____.
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   *Certified copies not received: _____

5. ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION. This three-month period for complying with the REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL is extendable under 37 CFR 1.136(a).**

6. ☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

7. ☐ Applicant MUST submit NEW FORMAL DRAWINGS

   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

   1) ☐ hereto or 2) ☐ to Paper No. _____.

   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the examiner.

   (c) ☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

8. ☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

1 ☐ Notice of References Cited (PTO-892)
2 ☐ Notice of Informal Patent Application (PTO-152)
3 ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
4 ☐ Interview Summary (PTO-413), Paper No. _____.
5 ☐ Information Disclosure Statement(s) (PTO-1449), Paper No(s). _____
6 ☐ Examiner's Amendment/Comment
7 ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
8 ☐ Examiner's Statement of Reasons for Allowance
9 ☐ Other

DANIEL H. PAN
PRIMARY EXAMINER
GROUP

NAK1-BG43 PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner: Pan, D
Heishi et al.	Group Art Unit: 2183
Serial No.: 09/280,777	April 23, 2001
Filed: March 29, 1999	Irvine, California 92614
For: INSTRUCTION CONVERTING APPARATUS USING PARALLEL EXECUTION CODE	

AMENDMENT

Honorable Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated February 14, 2001, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

In the Title of the Invention:

Please replace the Title of the Invention with:

--INSTRUCTION CONVERTING APPARATUS USING PARALLEL EXECUTION CODE--.

In the Claims:

Please cancel claims 2, 9, and 15 without prejudice or disclaimer of the subject matter contained therein.

Please amend the claims as follows:

1. (amended) An instruction conversion apparatus that converts an instruction sequence into parallel execution codes that are executable by a target processor, the target processor having predetermined limitations regarding combinations of instructions capable of being executed in parallel,

the instruction conversion apparatus comprising:

assigning means for successively assigning instructions in the instruction sequence to parallel execution codes; and

control means for controlling the assigning means so that a combination of a plurality of instructions that have already been assigned to a parallel execution code and an instruction that the assigning means is about to assign to the parallel execution code satisfy the predetermined limitations of the target processor;

wherein the target processor includes (1) a fetch means for successively fetching parallel execution codes that each include a plurality of unit fields from outside the target processor, (2) $s+k-1$ (where s,k are integers no smaller than 2) registers for storing $s+k-1$ unit fields included in at least two parallel execution codes that have been fetched by the fetch means, (3) decoding means, including s decoders that correspond to 1^{st} to s^{th} registers in the $s+k-1$ registers, the decoders decoding at least one opcode stored in any of the 1^{st} to s^{th} registers, and (4) operation executing means, connected to the $s+k-1$ registers for executing operations in accordance with a decoding result of the s decoders,

the assigning means assigning, when instructions to be assigned to a parallel execution code include a long instruction whose word length is equal to at least two but no more than k unit fields, one of an opcode and an operand of the long instruction to a u^{th} (where u is any integer such that $1<u<s$) unit field between the 1^{st} unit field and the s^{th} unit field, and only an operand of the long instruction to unit fields from a $(u+1)^{th}$ unit field to a $(u+k-1)^{th}$ unit field.

6. (amended) The instruction conversion apparatus of Claim 5, further comprising:

address resolving means for assigning a real address to a parallel execution code; and

second detecting means for detecting, when a real address has been assigned to a parallel execution code, an instruction including the real address that is not capable of being expressed by an original word length of the instruction,

the flag setting means setting the boundary flag at a unit field located one of before and after unit fields to which the instruction detected by the second detecting means has been assigned.

8. (amended) A processor, comprising:

fetch means for successively fetching parallel execution codes that include a plurality of unit fields from outside the processor;

a register set for storing a combination of a plurality of instructions included in at least two parallel execution codes that have been fetched by the fetch means;

decoding means for decoding, when the combination of instructions stored in the register set satisfies predetermined restrictions, the instructions in the combination in parallel; and

operation execution means for executing a plurality of operations in parallel in accordance with a decoding result of the decoding means;

s+k-1 (where *s,k* are integers no smaller than 2) registers for storing *s+k-1* unit fields included in at least two parallel execution codes that have been fetched by the fetch means,

the decoding means including *s* decoders that correspond to 1^{st} to s^{th} registers in the *s+k-1* registers and decode at least one opcode stored in any of the 1^{st} to s^{th} registers, and

the operation executing means being connected to the *s+k-1* registers and executing operations in accordance with a decoding result of the *s* decoders.

10. (amended) The processor of Claim 8,

wherein a long instruction whose word length is equal to at least two but no more than *k* unit fields is stored in any of the *s+k-1* registers with a first of the at least two but no more than *k* unit fields storing an opcode of the long instruction,

the decoding means including:

a decoding control unit which, when an opcode of a long instruction in stored in a u^{th} $(1<u<s)$ unit field between the 1^{st} unit field the s^{th} unit field, has the u^{th} decoder decode the opcode stored in the u^{th} register and a value stored between the u^{th} register and the $(u+k-1)^{th}$ register outputted to the operation execution means as an operand of the long instruction.

12. (amended) The processor of Claim 8,

wherein the decoding control unit performs control to invalidate a decoding operation of every decoder from the $(u+1)^{th}$ decoder onwards when a value stored between the $(u+1)^{th}$ register and the $(u+k-1)^{th}$ register is outputted to the operation execution means as an operand of a long instruction.

14. (amended) A computer-readable recording medium storing an instruction conversion program that converts an instruction sequence into parallel execution codes that are executable by a target processor, the target processor having predetermined limitations regarding combinations of instructions that can be executed in parallel,

the instruction conversion program comprising:

an assigning step for successively assigning instructions in the instruction sequence to parallel execution codes; and

a control step for controlling the assigning step so that a combination of a plurality of instructions that have already been assigned to a parallel execution code and an instruction that the assigning step is about to assign to the parallel execution code satisfy the predetermined limitations of the target processor;

wherein the target processor includes (1) a fetch means for successively fetching parallel execution codes that each include a plurality of unit fields from outside the target processor, (2) $s+k-1$ (where s,k are integers no smaller than 2) registers for storing $s+k-1$ unit fields included in at least two parallel execution codes that have been fetched by the fetch means, (3) decoding means, including s decoders that correspond to 1^{st} to s^{th} registers in the $s+k-1$ registers, the decoders decoding at least one opcode stored in any of

the 1^{st} to s^{th} registers, and (4) operation executing means, connected to the $s+k-1$ registers for executing operations in accordance with a decoding result of the s decoders,

the assigning step assigning, when instructions to be assigned to a parallel execution code include a long instruction whose word length is equal to at least two but no more than k unit fields, at least one of an opcode and an operand of the long instruction to a u^{th} (where u is any integer such that $1<u<s$) unit field between the 1^{st} unit field the s^{th} unit field, and only an operand of the long instruction to unit fields from a $(u+1)^{th}$ unit field to a $(u+k-1)^{th}$ unit field.

16. (amended) The computer-readable recording medium of Claim 14,

wherein the instruction conversion program further comprises:

a grouping step for forming an instruction group of a plurality of instructions that do not exhibit a dependency relation (hereafter "data dependency relation"), a data dependency relation being a relation between an instruction defining a resource and an instruction referring to the same resource; and

a first detecting step for detecting, when a 1^{st} to an s^{th} unit field in a parallel execution code have been assigned at least one instruction by the assigning step and an instruction (hereafter "short instruction") with a shorter word length than a long instruction is left in the instruction group, a long instruction assigned to unit fields between the 1^{st} unit field and the s^{th} unit field,

wherein the control step includes a first control substep for controlling the assigning step to rearrange instructions that have already been assigned to the parallel execution code so that the detected long instruction is assigned to unit fields between the s^{th} unit field and the $(s+k-1)^{th}$ unit field and the short instruction remaining in the

instruction group is assigned to a unit field between the 1^{st} unit field and the $(s-1)^{th}$ unit field.

Please add the following claims 21 - 36:

21. An instruction conversion apparatus that converts an instruction sequence into parallel execution codes that are executable by a target processor, the target processor having predetermined limitations regarding combinations of instructions capable of being executed in parallel,

the instruction conversion apparatus comprising:

an assigning unit for successively assigning instructions in the instruction sequence to parallel execution codes; and

a control unit for controlling the assigning unit so that a combination of a plurality of instructions that have already been assigned to a parallel execution code and an instruction that the assigning unit is about to assign to the parallel execution code satisfy the predetermined limitations of the target processor;

wherein the target processor includes (1) a fetch unit for successively fetching parallel execution codes that each include a plurality of unit fields from outside the target processor, (2) $s+k-1$ (where s,k are integers no smaller than 2) registers for storing $s+k-1$ unit fields included in at least two parallel execution codes that have been fetched by the fetch unit, (3) a decoding unit, including s decoders that correspond to 1^{st} to s^{th} registers in the $s+k-1$ registers, the decoders decoding at least one opcode stored in any of the 1^{st} to s^{th} registers, and (4) an operation executing unit, connected to the $s+k-1$ registers for executing operations in accordance with a decoding result of the s decoders,

the assigning unit assigning, when instructions to be assigned to a parallel execution code include a long instruction whose word length is equal to at least two but no more than *k* unit fields, one of an opcode and an operand of the long instruction to a u^{th} (where *u* is any integer such that $1<u<s$) unit field between the 1^{st} unit field and the s^{th} unit field, and only an operand of the long instruction to unit fields from a $(u+1)^{th}$ unit field to a $(u+k-1)^{th}$ unit field.

22. The instruction conversion apparatus of Claim 21, further comprising:

a grouping unit for forming an instruction group of a plurality of instructions that do not exhibit a dependency relation (hereafter "data dependency relation"), a data dependency relation being a relation between an instruction defining a resource and an instruction referring to the same resource; and

a first detecting unit for detecting, when a 1^{st} to an s^{th} unit field in a parallel execution code have been assigned at least one instruction by the assigning unit and an instruction (hereafter "short instruction") with a shorter word length than a long instruction is left in the instruction group, a long instruction assigned to unit fields between the 1^{st} unit field and the s^{th} unit field,

wherein the control unit includes a first control unit for controlling the assigning unit to rearrange instructions that have already been assigned to the parallel execution code so that the detected long instruction is assigned to unit fields between the s^{th} unit field and the $(s+k-1)^{th}$ unit field and the short instruction remaining in the instruction group is assigned to a unit field between the 1^{st} unit field and the $(s-1)^{th}$ unit field.

23. The instruction conversion apparatus of Claim 22,

wherein the instruction group includes instructions that exhibit an anti-dependence and instructions that exhibit an output dependence, an anti-dependence being a relation between an instruction that refers to a resource and an instruction that thereafter defines the resource, and an output dependence being a relation between an instruction that defines a resource and another instruction that defines the resource,

the control unit including a search unit for searching for a combination pattern, composed of a plurality of instructions in the instruction group, that is unaffected by an anti-dependence and an output dependence, and

the first control unit controlling the assigning unit to rearrange the plurality of instructions in accordance with the combination pattern found by the search unit, to assign the long instruction found by the detecting unit to unit fields from the s^{th} unit field to the $(s+k-1)^{th}$ unit field, and to assign a short instruction left in the instruction group to a unit field between the 1^{st} unit field and the $(s-1)^{th}$ unit field.

24. The instruction conversion apparatus of Claim 23, further comprising:

a flag setting unit for setting a parallel execution boundary flag at each boundary that marks a position at which the predetermined limitations of the target processor dictate that parallel execution is not possible.

25. The instruction conversion apparatus of Claim 24, further comprising:

an address resolving unit for assigning a real address to a parallel execution code; and

a second detecting unit for detecting, when a real address has been assigned to a parallel execution code, an instruction including the real address that is not capable of being expressed by an original word length of the instruction,

the flag setting unit setting the boundary flag at a unit field located one of before and after unit fields to which the instruction detected by the second detecting unit has been assigned.

26. The instruction conversion apparatus of Claim 25, further comprising:

a replacing unit for replacing an instruction detected by the second detecting unit with a transfer instruction that transfers an address to a register and an addressing instruction that performs the same processing as the replaced instruction using the register,

the assigning unit assigning the two instructions substituted by the replacing unit to a plurality of unit fields, and

the flag setting unit setting a boundary flag at one of the plurality of unit fields to which the two substituted instructions have been assigned to show a parallel execution boundary.

27. A processor, comprising:

a fetch unit for successively fetching parallel execution codes that include a plurality of unit fields from outside the processor;

a register set for storing a combination of a plurality of instructions included in at least two parallel execution codes that have been fetched by the fetch unit;

a decoding unit for decoding, when the combination of instructions stored in the register set satisfies predetermined restrictions, the instructions in the combination in parallel; and

an operation execution unit for executing a plurality of operations in parallel in accordance with a decoding result of the decoding unit;

s+k-1 (where *s,k* are integers no smaller than 2) registers for storing *s+k-1* unit fields included in at least two parallel execution codes that have been fetched by the fetch unit,

the decoding unit including *s* decoders that correspond to 1^{st} to s^{th} registers in the *s+k-1* registers and decode at least one opcode stored in any of the 1^{st} to s^{th} registers, and

the operation executing unit being connected to the *s+k-1* registers and executing operations in accordance with a decoding result of the *s* decoders.

28. The processor of Claim 27,

wherein a long instruction whose word length is equal to at least two but no more than *k* unit fields is stored in any of the *s+k-1* registers with a first of the at least two but no more than *k* unit fields storing an opcode of the long instruction,

the decoding unit including:

a decoding control unit which, when an opcode of a long instruction in stored in a u^{th} $(1<u<s)$ unit field between the 1^{st} unit field the s^{th} unit field, has the u^{th} decoder decode the opcode stored in the u^{th} register and a value stored between the u^{th} register and the $(u+k-1)^{th}$ register outputted to the operation execution unit as an operand of the long instruction.

29. The processor of Claim 27

wherein the decoding control unit performs control to invalidate a decoding operation of every decoder from the $(u+1)^{th}$ decoder onwards when a value stored between the $(u+1)^{th}$ register and the $(u+k-1)^{th}$ register is outputted to the operation execution unit as an operand of a long instruction.

30. A recording medium storing executable code for a processor, the processor including (1) a fetch unit for successively fetching parallel execution codes that each include a plurality of unit fields from outside the target processor, (2) $s+k-1$ (where s,k are integers no smaller than 2) registers for storing $s+k-1$ unit fields included in at least two parallel execution codes that have been fetched by the fetch unit, (3) a decoding unit, including s decoders that correspond to 1^{st} to s^{th} registers in the $s+k-1$ registers, the decoders decoding at least one opcode stored in any of the 1^{st} to s^{th} registers, and (4) an operation executing unit, connected to the $s+k-1$ registers for executing operations in accordance with a decoding result of the s decoders,

the executable code stored on the recording medium being arranged such that at least one of an opcode and an operand of a long instruction having a word length of at least two but no more than k unit fields is arranged into to a u^{th} (where u is any integer such that $1<u<s$) unit field between the 1^{st} unit field and the s^{th} unit field and the s^{th} unit field, and only an operand of the long instruction is arranged in unit fields from a $(u+1)^{th}$ unit field to a $(u+k-1)^{th}$ unit field.

31. A computer-readable recording medium storing an instruction conversion program that converts an instruction sequence into parallel execution codes that are

executable by a target processor, the target processor having predetermined limitations regarding combinations of instructions that can be executed in parallel,

the instruction conversion program comprising:

an assigning step for successively assigning instructions in the instruction sequence to parallel execution codes; and

a control step for controlling the assigning step so that a combination of a plurality of instructions that have already been assigned to a parallel execution code and an instruction that the assigning step is about to assign to the parallel execution code satisfy the predetermined limitations of the target processor;

wherein the target processor includes (1) a fetch unit for successively fetching parallel execution codes that each include a plurality of unit fields from outside the target processor, (2) $s+k-1$ (where s,k are integers no smaller than 2) registers for storing $s+k-1$ unit fields included in at least two parallel execution codes that have been fetched by the fetch unit, (3) a decoding unit, including s decoders that correspond to 1^{st} to s^{th} registers in the $s+k-1$ registers, the decoders decoding at least one opcode stored in any of the 1^{st} to s^{th} registers, and (4) an operation executing unit, connected to the $s+k-1$ registers for executing operations in accordance with a decoding result of the s decoders,

the assigning step assigning, when instructions to be assigned to a parallel execution code include a long instruction whose word length is equal to at least two but no more than k unit fields, at least one of an opcode and an operand of the long instruction to a u^{th} (where u is any integer such that $1<u<s$) unit field between the 1^{st} unit field the s^{th} unit field, and only an operand of the long instruction to unit fields from a $(u+1)^{th}$ unit field to a $(u+k-1)^{th}$ unit field.

32. The computer-readable recording medium of Claim 31,

wherein the instruction conversion program further comprises:

a grouping step for forming an instruction group of a plurality of instructions that do not exhibit a dependency relation (hereafter "data dependency relation"), a data dependency relation being a relation between an instruction defining a resource and an instruction referring to the same resource; and

a first detecting step for detecting, when a 1^{st} to an s^{th} unit field in a parallel execution code have been assigned at least one instruction by the assigning step and an instruction (hereafter "short instruction") with a shorter word length than a long instruction is left in the instruction group, a long instruction assigned to unit fields between the 1^{st} unit field and the s^{th} unit field,

wherein the control step includes a first control substep for controlling the assigning step to rearrange instructions that have already been assigned to the parallel execution code so that the detected long instruction is assigned to unit fields between the s^{th} unit field and the $(s+k-1)^{th}$ unit field and the short instruction remaining in the instruction group is assigned to a unit field between the 1^{st} unit field and the $(s-1)^{th}$ unit field.

33. The computer-readable recording medium of Claim 32,

wherein the instruction group includes instructions that exhibit an anti-dependence and instructions that exhibit an output dependence, an anti-dependence being a relation between an instruction that refers to a resource and an instruction that thereafter defines the resource, and an output dependence being a relation between an instruction that defines a resource and another instruction that defines the resource,

the control step including a search substep for searching for a combination pattern, composed of a plurality of instructions in the instruction group, that is unaffected by an anti-dependence and an output dependence, and

the first control substep controlling the assigning step to rearrange the plurality of instructions in accordance with the combination pattern found by the search substep, to assign the long instruction found by the detecting step to unit fields from the s^{th} unit field to the $(s+k-1)^{th}$ unit field, and to assign a short instruction left in the instruction group to a unit field between the 1^{st} unit field and the $(s-1)^{th}$ unit field.

34. The computer-readable recording medium of Claim 33,

wherein the instruction conversion program further comprises:

a flag setting step for setting a parallel execution boundary flag at each boundary that marks a position at which the predetermined limitations of the target processor dictate that parallel execution is not possible.

35. The computer-readable recording medium of Claim 34,

wherein the instruction conversion program further comprises:

an address resolving step for assigning a real address to a parallel execution code; and

a second detecting step for detecting, when a real address has been assigned to a parallel execution code, an instruction including the real address that cannot be expressed by an original word length of the instruction,

the flag setting step setting the boundary flag at a unit field located one of before and after unit fields to which the instruction detected by the second detecting step has been assigned.

36. The computer-readable recording medium of Claim 35,

wherein the instruction conversion program further comprises:

a replacing step for replacing an instruction detected by the second detecting step with a transfer instruction that transfers an address to a register and an addressing instruction that performs the same processing as the replaced instruction using the register,

the assigning step assigning the two instructions substituted by the replacing step to a plurality of unit fields, and

the flag setting step setting a boundary flag at one of the plurality of unit fields to which the two substituted instructions have been assigned to show a parallel execution boundary.

REMARKS

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

This amendment is responsive to the Office Action dated February 14, 2001. In the application Claims 1 – 20 were pending, and the Office Action rejected Claims 1, 8, and 14 pursuant to Title 35 U.S.C. §103 as being obvious over Umekita (5,452,461) in view of Hertile (3,955,180). The Office Action noted some minor syntax errors that have been corrected with the assistance of the Examiner's helpful suggestions.

Claims 2 – 7, 9 – 12, and 15 – 20 were deemed to contain allowable subject matter but were objected to for depending from rejected claims. Claim 13 was allowed. Applicants would initially like to thank the Examiner for his helpful suggestions with respect to the application and for the indication of allowable subject matter. Without acquiescing to the rejections in the Office Action, Applicants have modified Claims 1, 8 and 14 to include the allowable subject matter of the claims immediately following said claims, and canceled the duplicative claims.

Additionally, Applicants have added a new set of claims that substitute the term "means" in the original set of claims with "unit" so as not to implicate Title 35 U.S.C. §112 paragraph 6. The new set of claims include the allowable subject matter of the previously identified claims and are believed to be allowable on this basis. Accordingly, Applicants believe that the application is now in condition for allowance.

If the Examiner feels that a telephone interview will further the prosecution of this case, the Examiner is invited to contact the Applicants at the number below.

Respectfully submitted,

PRICE AND GESS

By: Michael J. Moffatt

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2100 S.E. Main St., Suite 250
Irvine, California 92614
Telephone: 949/261-8433

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington DC 20231
on April 23, 2001
Daniel Kerby
Signature
April 23, 2001
Date

Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 2, 9, and 15 have been canceled.

The Claims have been amended as follows:

1. (amended) An instruction conversion apparatus that converts an instruction sequence into parallel execution codes that are executable by a target processor, the target processor having predetermined limitations regarding combinations of instructions [that can be] capable of being executed in parallel,

the instruction conversion apparatus comprising:

assigning means for successively assigning instructions in the instruction sequence to parallel execution codes; and

control means for controlling the assigning means so that a combination of a plurality of instructions that have already been assigned to a parallel execution code and an instruction that the assigning means is about to assign to the parallel execution code satisfy the predetermined limitations of the target processor[.];

wherein the target processor includes (1) a fetch means for successively fetching parallel execution codes that each include a plurality of unit fields from outside the target processor, (2) $s+k-1$ (where s,k are integers no smaller than 2) registers for storing $s+k-1$ unit fields included in at least two parallel execution codes that have been fetched by the fetch means, (3) decoding means, including s decoders that correspond to 1^{st} to s^{th} registers in the $s+k-1$ registers, the decoders decoding at least one opcode stored in any of the 1^{st} to s^{th} registers, and (4) operation executing means, connected to the $s+k-1$ registers for executing operations in accordance with a decoding result of the s decoders.

the assigning means assigning, when instructions to be assigned to a parallel execution code include a long instruction whose word length is equal to at least two but no more than k unit fields, one of an opcode and an operand of the long instruction to a u^{th} (where u is any integer such that $1<u<s$) unit field between the 1^{st} unit field and the s^{th} unit field, and only an operand of the long instruction to unit fields from a $(u+1)^{th}$ unit field to a $(u+k-1)^{th}$ unit field.

6. (amended) The instruction conversion apparatus of Claim 5, further comprising:

address resolving means for assigning a real address to a parallel execution code; and

second detecting means for detecting, when a real address has been assigned to a parallel execution code, an instruction including the real address that [cannot be] is not capable of being expressed by an original word length of the instruction,

the flag setting means setting the boundary flag at a unit field located one of before and after unit fields to which the instruction detected by the second detecting means has been assigned.

8. (amended) A processor, comprising:

fetch means for successively fetching parallel execution codes that include a plurality of unit fields from outside the processor;

a register set for storing a combination of a plurality of instructions included in at least two parallel execution codes that have been fetched by the fetch means;

decoding means for decoding, when the combination of instructions stored in the register set satisfies predetermined restrictions, the instructions in the combination in parallel; and

operation execution means for executing a plurality of operations in parallel in accordance with a decoding result of the decoding means[.];

s+k-1 (where *s,k* are integers no smaller than 2) registers for storing *s+k-1* unit fields included in at least two parallel execution codes that have been fetched by the fetch means,

the decoding means including *s* decoders that correspond to 1^{st} to s^{th} registers in the *s+k-1* registers and decode at least one opcode stored in any of the 1^{st} to s^{th} registers, and

the operation executing means being connected to the *s+k-1* registers and executing operations in accordance with a decoding result of the *s* decoders.

10. (amended) The processor of Claim [9]8,

wherein a long instruction whose word length is equal to at least two but no more than *k* unit fields is stored in any of the *s+k-1* registers with a first of the at least two but no more than *k* unit fields storing an opcode of the long instruction,

the decoding means including:

a decoding control unit which, when an opcode of a long instruction in stored in a u^{th} $(1<u<s)$ unit field between the 1^{st} unit field the s^{th} unit field, has the u^{th} decoder decode the opcode stored in the u^{th} register and a value stored between the u^{th} register and the $(u+k-1)^{th}$ register outputted to the operation execution means as an operand of the long instruction.

12. (amended) The processor of Claim [9]8,

wherein the decoding control unit performs control to invalidate a decoding operation of every decoder from the $(u+1)^{th}$ decoder onwards when a value stored between the $(u+1)^{th}$ register and the $(u+k-1)^{th}$ register is outputted to the operation execution means as an operand of a long instruction.

14. (amended) A computer-readable recording medium storing an instruction conversion program that converts an instruction sequence into parallel execution codes that are executable by a target processor, the target processor having predetermined limitations regarding combinations of instructions that can be executed in parallel,

the instruction conversion program comprising:

an assigning step for successively assigning instructions in the instruction sequence to parallel execution codes; and

a control step for controlling the assigning step so that a combination of a plurality of instructions that have already been assigned to a parallel execution code and an instruction that the assigning step is about to assign to the parallel execution code satisfy the predetermined limitations of the target processor[.];

wherein the target processor includes (1) a fetch means for successively fetching parallel execution codes that each include a plurality of unit fields from outside the target processor, (2) $s+k-1$ (where s,k are integers no smaller than 2) registers for storing $s+k-1$ unit fields included in at least two parallel execution codes that have been fetched by the fetch means, (3) decoding means, including s decoders that correspond to 1^{st} to s^{th} registers in the $s+k-1$ registers, the decoders decoding at least one opcode stored in any of

the 1^{st} to s^{th} registers, and (4) operation executing means, connected to the $s+k-1$ registers for executing operations in accordance with a decoding result of the s decoders,

the assigning step assigning, when instructions to be assigned to a parallel execution code include a long instruction whose word length is equal to at least two but no more than k unit fields, at least one of an opcode and an operand of the long instruction to a u^{th} (where u is any integer such that $1<u<s$) unit field between the 1^{st} unit field the s^{th} unit field, and only an operand of the long instruction to unit fields from a $(u+1)^{th}$ unit field to a $(u+k-1)^{th}$ unit field.

16. (amended) The computer-readable recording medium of Claim [15]14,

wherein the instruction conversion program further comprises:

a grouping step for forming an instruction group of a plurality of instructions that do not exhibit a dependency relation (hereafter "data dependency relation"), a data dependency relation being a relation between an instruction defining a resource and an instruction referring to the same resource; and

a first detecting step for detecting, when a 1^{st} to an s^{th} unit field in a parallel execution code have been assigned at least one instruction by the assigning step and an instruction (hereafter "short instruction") with a shorter word length than a long instruction is left in the instruction group, a long instruction assigned to unit fields between the 1^{st} unit field and the s^{th} unit field,

wherein the control step includes a first control substep for controlling the assigning step to rearrange instructions that have already been assigned to the parallel execution code so that the detected long instruction is assigned to unit fields between the s^{th} unit field and the $(s+k-1)^{th}$ unit field and the short instruction remaining in the

instruction group is assigned to a unit field between the 1^{st} unit field and the $(s-1)^{th}$ unit field.

Claims 21 - 35 have been added.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/280,277	03/29/99	HELLER	NAK1-5003

EXAMINER

JOSEPH W PRICE
PRICE GESS & UBELL
2100 S E MAIN STREET STE 250
IRVINE CA 92614

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 02/14/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

RESPONSE DUE 5-14-01
ACTION Amendment

RECEIVED
FEB 20 2001
PRICE AND GESS

MH

Office Action Summary	Application No. 09/280,777	Applicant(s) Helshi et al.
	Examiner Pan	Group Art Unit 2183

☒ Responsive to communication(s) filed on *Mar 29, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-20* is/are pending in the applicat

Of the above, claim(s) *none* is/are withdrawn from consideration

☒ Claim(s) *13* is/are allowed.

☒ Claim(s) *1, 8, and 14* is/are rejected.

☒ Claim(s) *2-7, 9-12, and 15-20* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948. (Not objected)

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

DANIEL H. PAN
PRIMARY EXAMINER
GROUP

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

1. Claims 1-20 are presented for examination.

2. Applicant is kindly suggested to reduce the lengthy title.

3. Claims 1-7,14-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. As to claim 1, line 5, "can be" is indefinite. Suggestion : able to, capable of, or the like. See also claim 14, line 6.

5. As to claim 6, line 7, "cannot be" is indefinite. Suggestion : not able to, not capable of, or the like.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Umekita (5,452,461) in view of Hertile (3,955,180) .

7. As to claims 1,14, Umekita disclosed an instruction conversion system comprising at least :

a) assigning means [table] for assigning instructions on the instruction sequence [virtual code] to parallel codes [real code] (e.g., col.7, lines 50-65).

8. Umekita did not specifically show the control means for controlling the assigned instructions and the instruction was about to assigned to the parallel codes satisfied a predetermined limitations of the target processor as claimed. However, Hertile disclosed a system including predetermined target processor limitations (e.g. see col.1, lines 40-45, lines 65-68, col.2, lines 1-7). It would have been obvious to one of ordinary skill in the art to use Hertile in Umekita for including the control means as claimed because the use of Hertile could provide enhanced control for assigning the instruction sequence in Umekita to adjust to specific requirements of the execution of the parallel codes in the target processor.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. (4,858,105) in view of Suko et al. (4,611,281).

As to claim 8, Kuriyama disclosed at least :

a)fetching means (see col.12, lines 43-47) for fetching a instruction codes in parallel ;

b)decoding means (col.1, lines 45-50, col.13, lines 5-14) for decoding the instructions in parallel ;

c)operation execution means for executing the plurality of operations in parallel based on the decoding result (e.g. see col.1, lines 60-68, col.2, lines 1-2, col.13, lines 5-14).

10. Kuriyama did not specifically show the register set for storing combination of the plurality of instructions included in the parallel instruction codes as claimed. However, Suko disclosed a system including a register set [trace memory] for storing a combination of data corresponding to a plurality of instructions (col.4, lines 13-23, col.5, lines 42-47. It would have been obvious to one of ordinary skill in the art to use Suko in Kuriyama for storing the combination of the plurality of

instructions as claimed because the use of Suko could increase the adaptability of Kuriyama to accept a combination set of plurality of instructions in a given storage.

11. Claim 13 is allowable over the art of record.

12. Claims 2-7,9-12,15-20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to d Pan whose telephone number is (703) 305 9696. The examiner can normally be reached on M-F from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chang, can be reached on (703) 305 3900. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 6306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

DANIEL D. PAN
PRIMARY EXAMINER
GROUP

Notice of References Cited

Application No.	Applicant(s)		
09/280,777	Heishi et al.		
Examiner		Group Art Unit	Page 1 of 1
Pan		2183	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	4,611,281	09/09/86	Suko Et A.	714	39
	B	4,858,105	08/15/89	Kuriyama et al.	712	235
	C	3,955,180	05/04/76	Hirtle	703	26
	D	5,452,461	09/09/86	Umekita et'al.	717	6
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U		
	V		
	W		
	X		

69 / 290,377

Form PTO 948 (Rev. 8-98) U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office Application No.

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 3/30/09 are:

A. ☒ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☐ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be sumitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ___ Color drawings are not acceptable until petition is granted. Fig(s) ___
   - ___ Pencil and non black ink not permitted. Fig(s) ___
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
   - ___ 1 full-tone set is required. Fig(s) ___
   - ___ Photographs not properly mounted (must use brystol board or photographic double-weight paper). Fig(s) ___
   - ___ Poor quality (half-tone). Fig(s) ___
3. TYPE OF PAPER. 37 CFR 1.84(e)
   - ___ Paper not flexible, strong, white, and durable. Fig(s) ___
   - ___ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) ___
   - ___ Mylar, velum paper is not acceptable (too thin). Fig(s) ___
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   - ___ 21.0 cm by 29.7 cm (DIN size A4)
   - ___ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   - ___ All drawing sheets not the same size. Sheet(s) ___
   - ___ Drawings sheets not an acceptable size. Fig(s) ___
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

   Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size

   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8.1/2 x 11

   Margins not acceptable. Fig(s) ___

   ___ Top (T) ___ Left (L)
   ___ Right (R) ___ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)

   REMINDER: Specification may require revision to correspond to drawing changes.

   Partial views. 37 CFR 1.84(h)(2)
   - ___ Brackets needed to show figure as one entity. Fig(s) ___
   - ___ Views not labeled separately or properly. Fig(s) ___
   - ___ Enlarged view not labeled separately or properly. Fig(s) ___
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   - ___ Hatching not indicated for sectional portions of an object. Fig(s) ___
   - ___ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) ___
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) ___
9. SCALE. 37 CFR 1.84(k)
   - ___ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) ___
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(j)
    - ___ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) ___
11. SHADING. 37 CFR 1.84(m)
    - ___ Solid black areas pale. Fig(s) ___
    - ___ Solid black shading not permitted. Fig(s) ___
    - ___ Shade lines, pale, rough and blurred. Fig(s) ___
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
    - ___ Numbers and reference characters not plain and legible. Fig(s) ___
    - ___ Figure legends are poor. Fig(s) ___
    - ___ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) ___
    - ___ English alphabet not used. 37 CFR 1.84(p)(2) Figs ___
    - ___ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) ___
13. LEAD LINES. 37 CFR 1.84(q)
    - ___ Lead lines cross each other. Fig(s) ___
    - ___ Lead lines missing. Fig(s) ___
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    - ___ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) ___
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    - ___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) ___
16. CORRECTIONS. 37 CFR 1.84(w)
    - ___ Corrections not made from prior PTO-948 dated ___
17. DESIGN DRAWINGS. 37 CFR 1.152
    - ___ Surface shading shown not appropriate. Fig(s) ___
    - ___ Solid black shading not used for color contrast. Fig(s) ___

COMMENTS

REVIEWER Tarry DATE 3/20/09 TELEPHONE NO. ___

ATTACHMENT TO PAPER NO. ___